IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

GODEFRIDUS A.M. HURKX ET AL | PHN 16,741A

Serial No. | Prior Group Art Unit: 2815

Filed: Concurrently | Prior Examiner: M. Warren

SEMICONDUCTOR DEVICE WITH A BIPOLAR TRANSISTOR, AND METHOD OF MANUFACTURING SUCH A METHOD

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claims 1-5 and amend claims 6-10 as follows:

6. (Amended) A method of manufacturing a semiconductor device whereby a first semiconductor region is formed in a semiconductor body comprising a substrate, which first semiconductor region lies in the semiconductor body, is of a first conductivity type, forms a collector region of a bipolar transistor, and is provided with a first connection conductor, whereby a second semiconductor region of a second conductivity type opposed to the first is formed above said first semiconductor region, which second semiconductor region forms a base region of the transistor, adjoins the surface of the semiconductor body, and is provided with a second connection conductor at said surface, and whereby a third semiconductor region is formed which is recessed into the second semiconductor

region, which is of the first conductivity type, which forms an emitter region of the transistor, and which is provided with a third connection conductor, and whereby the device is provided with means for preventing a saturation of the transistor during normal use, characterized in that the second connection conductor is exclusively connected to the second semiconductor region for preventing a saturation of the transistor, and in that a partial region of that portion of the second semiconductor region which lies outside the third semiconductor region, as seen in projection, and adjacent the second connection conductor is provided with a smaller flux of dopant atoms.

7. (Amended) A method as claimed in claim 6, characterized in that the partial region of the second semiconductor region is formed below the second connection conductor and is given a smaller thickness and a lower doping concentration.

8. (Amended) A method as claimed in claim 6, characterized in that the partial region of the second semiconductor region is given a smaller thickness.

9. (Amended) A method as claimed in claim 6, characterized in that the partial region of the second semiconductor region is formed by means of ion implantation.

10. (Amended) A method as claimed in claim 6, characterized in that a thin, strongly doped fourth semiconductor region of the first conductivity type is formed between the partial region of the second semiconductor region and the second connection conductor, preferably simultaneously with the third semiconductor region.

IN THE ABSTRACT

Please delete the abstract in its entirety and replace with the following:

--ABSTRACT OF THE DISCLOSURE

The invention relates to a semiconductor device including a preferably discrete bipolar transistor with a collector region, a base region, and an emitter region which are provided with connection conductors. A known means of preventing a saturation of the transistor is that the latter is provided with a Schottky clamping diode. The latter is formed in that case in that the connection conductor of the base region is also put into contact with the collector region. In a device according to the invention, the second connection conductor is exclusively connected to the base region, and a partial region of that portion of the base region which lies outside the emitter region, as seen in projection, lying below the second connection conductor is given a smaller flux of dopant atoms. The bipolar transistor in a device according to the invention is provided with a pn clamping diode which is formed between the partial region and the collector region. Such a device has excellent properties, such as a short switching time and a saturation collector-emitter voltage which is not too high, while having a low, non-variable and well reproducible leakage current, unlike the known device. The reduced flux of dopant atoms of the partial region is preferably realized in that the partial region is given a smaller doping concentration and/or thickness than the remainder of the portion of the base region which lies outside the emitter region. In a favourable modification, a region provided simultaneously with the emitter region is present between the partial region and the second connection conductor.--.

REMARKS

The claims have been amended to delete multiple dependencies and parenthetical reference. The abstract has been amended. Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

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May 10, 2001

APPENDIX

6. (Amended) A method of manufacturing a semiconductor device whereby a first semiconductor region ~~(1)~~ is formed in a semiconductor body ~~(10)~~ comprising a substrate ~~(11)~~, which first semiconductor region ~~(1)~~ lies in the semiconductor body ~~(10)~~, is of a first conductivity type, forms a collector region of a bipolar transistor, and is provided with a first connection conductor ~~(6)~~, whereby a second semiconductor region ~~(2)~~ of a second conductivity type opposed to the first is formed above said first semiconductor region ~~(1)~~, which second semiconductor region ~~(2)~~ forms a base region of the transistor, adjoins the surface of the semiconductor body ~~(10)~~, and is provided with a second connection conductor ~~(7)~~ at said surface, and whereby a third semiconductor region ~~(3)~~ is formed which is recessed into the second semiconductor region ~~(2)~~, which is of the first conductivity type, which forms an emitter region of the transistor, and which is provided with a third connection conductor ~~(8)~~, and whereby the device is provided with means for preventing a saturation of the transistor during normal use, characterized in that the second connection conductor ~~(7)~~ is exclusively connected to the second semiconductor region ~~(2)~~ for preventing a saturation of the transistor, and in that a partial region ~~(2B)~~ of that portion ~~(2A)~~ of the second semiconductor region ~~(2)~~ which lies outside the third semiconductor region ~~(3)~~, as seen in projection, and adjacent the second connection conductor ~~(7)~~ is provided with a smaller flux of dopant atoms.

7. (Amended) A method as claimed in claim 6, characterized in that the partial region ~~(2B)~~ of the second semiconductor region ~~(2)~~ is formed below the second connection conductor ~~(7)~~ and is given a smaller thickness and a lower doping concentration.

8. (Amended) A method as claimed in claim 6 ~~or 7~~, characterized in that the partial region ~~(2B)~~ of the second semiconductor region ~~(2)~~ is given a smaller thickness.

9. (Amended) A method as claimed in claim 6, ~~7 or 8,~~ characterized in that the partial region ~~(2B)~~ of the second semiconductor region ~~(2)~~ is formed by means of ion implantation.

10. (Amended) A method as claimed in claim 6, ~~7, 8 or 9,~~ characterized in that a thin, strongly doped fourth semiconductor region ~~(4)~~ of the first conductivity type is formed between the partial region ~~(2B)~~ of the second semiconductor region ~~(2)~~ and the second connection conductor ~~(7)~~, preferably simultaneously with the third semiconductor region ~~(3)~~.